

### **REMARKS**

Claims 1, 3, and 5-9 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

### **PRIORITY**

The Examiner asserts that to obtain the benefit of foreign priority under 35 U.S.C. 119(a) – (d) prior to declaration of an interference, a certified English translation of the foreign application must be submitted in reply to this action. Applicant respectfully disagrees. Under 37 C.F.R. § 1.55(a)(4)(i), an English language translation of a non-English language foreign application is not required.

### **CLAIM OBJECTIONS**

The objection to claim 2 is rendered moot by cancellation.

### **REJECTION UNDER 35 U.S.C. § 103**

Claims 1-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ikeda et al. (U.S. Pub. No. 2001/0011988 A1) in view of Priem et al. (U.S. Pat. No. 5,805,133). With respect to claims 2 and 4, the rejection is rendered moot by cancellation. With respect to claims, 1, 3, and 5-9, the rejection is respectfully traversed.

Claim 1 recites a display driver for driving data lines of an electro optic device based on display data. A display data random access memory includes a plurality of word lines, a plurality of column lines, and a plurality of memory cells each storing

display data of one pixel. A display address decoder selects a word line of the display data random access memory based on a display address. A display column address decoder selects a column line of the display data random access memory based on a display column address. A plurality of read-out bit lines are each commonly coupled to a memory cell group specified by a corresponding column line. A scroll bus is coupled to the plurality of read-out bit lines. A shift register outputs a shift output shifted based on a given shift clock. The shift register includes a plurality of shift register latches. A line latch loads display data that are loaded in the plurality of data latches in one horizontal scan cycle. A plurality of data latches each corresponds to each data line of the electro optic device and loads display data on the scroll bus. Each data latch is connected to the line latch and to a shift register latch of the plurality of shift register latches. A driving circuit drives the data lines based on the display data loaded in the plurality of data latches. Display data of one pixel is read out from a memory cell specified by a word line selected by the display address decoder and a column line selected by the display column address decoder. The data are output to the scroll bus via the read-out bit line coupled to the memory cell. The data on the scroll bus are loaded in each of the plurality of data latches. Each of the plurality of data latches loads display data on the scroll bus based on the shift output of each stage of the shift register. An image generated by loading the display data is scrolled in an oblique direction to upper right, upper left, lower right, and lower left by combining vertical scrolling and horizontal scrolling based on the data output to the scroll bus and based on the shift output of each stage of the shift register. Ikeda et al. and Priem et al. fail to teach or suggest the display driver recited by claim 1.

Ikeda et al. describes an information processing system with a bus, a display data generating circuit, and a display apparatus with a display panel capable of displaying a gray scale image in accordance with display data in a form of a plurality of bits for each of a plurality of pixels of a display panel. Ikeda et al., Abstract. As noted by the Examiner, Ikeda et al. fails to teach a plurality of readout bit lines, a scroll bus, a plurality of data latches, and a driving circuit. Priem et al. is cited for the missing limitations. The Examiner, however, has not explained how the information processing

system of Ikeda et al. may be combined with the frame buffer and memory array of Priem et al. to arrive at the display driver recited by claim 1.

Moreover, both Ikeda et al. and Priem et al. are silent as to the specific display driver structure recited by claim 1, including the shift register, the line latch, and the plurality of data latches with each data latch being connected to the line latch and to a shift register latch of the plurality of shift register latches. In addition, Ikeda et al. and Priem et al. are silent as to an image generated by loading the display data being scrolled in an oblique direction to upper right, upper left, lower right, and lower left by combining vertical scrolling and horizontal scrolling based on the data output to the scroll bus and based on the shift output of each stage of the shift register.

For these reasons, Ikeda et al. and Priem et al. fail to teach or suggest the display driver recited by claim 1. Applicant notes that claims 3 and 5-7 each depend either directly or indirectly from claim 1 which defines over the prior art as discussed above. For at least the above reasons, claims 3 and 5-7 likewise define over the prior art. Reconsideration and withdrawal of the rejections are respectfully requested.

With respect to claim 8, a display driving method for driving data lines of an electro optic device based on display data that are read out from a display data random access memory including a plurality of word lines, a plurality of column lines, and a plurality of memory cells each storing display data of one pixel is recited. The method comprises specifying a memory cell by a word line out of the plurality of word lines and a column line out of the plurality of column lines. The method also comprises outputting display data of one pixel that are stored in the memory cell to a scroll bus via a read-out bit line commonly coupled to a memory cell group that is specified by the column line. The method also comprises outputting a shift output shifted based on a given shift clock with a shift register including a plurality of shift register latches. The method also comprises loading the display data of one pixel on the scroll bus in any of a plurality of data latches each corresponding to each data line of the electro optic device, each data latch being connected to a line latch and to a shift register latch of said plurality of shift register latches. The method also comprises driving the data lines of the electro optic device based on the display data loaded in the plurality of data latches. An image generated by loading the display data is scrolled in an oblique direction to upper right,

upper left, lower right, and lower left by combining vertical scrolling and horizontal scrolling based on the shift output of each stage of the shift register.

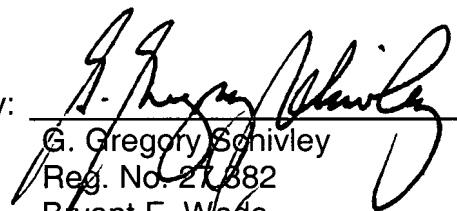
Similar limitations are recited by claim 1. For at least the above reasons, Ikeda et al. and Priem et al. fail to teach or suggest the method recited by claim 8. Applicant notes that claim 9 depends from claim, which defines over the prior art as discussed above. Claim 9 likewise defines over the prior art. Reconsideration and withdrawal of the rejections are respectfully requested.

### CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: Aug 3, 2007

By:   
G. Gregory Schivley  
Reg. No. 27,882  
Bryant E. Wade  
Reg. No. 40,344

HARNESS, DICKEY & PIERCE, P.L.C.  
P.O. Box 828  
Bloomfield Hills, Michigan 48303  
(248) 641-1600

GGG/BEW/MPD/mmk